31.1 A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process

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The recent advent of WPAN standards [1] using high signal bandwidths has necessitated the design of high-speed low-power ADCs. Recently, a lot of effort has been put into exploring architectures to reduce power consumption of high-speed low-resolution converters, e.g., a parallel SAR array [2], a pipeline ADC [3], and low-power flash converters [4]. The lowest reported energy per conversion-step is 0.5pJ [2]. In this paper, a high-speed 4b flash ADC in 90nm digital CMOS is presented. It achieves 1.25GS/s sampling rate and 3.7 ENOB from DC to Nyquist signal bandwidth while consuming 2.5mW that results in an energy per conversion-step of 0.16pJ.

In this ADC, to save power, all the non-essential blocks of the flash architecture have been removed (see Fig. 31.1.1). These non-essential blocks are: T/H, preamplifiers, reference ladder, and bubble error correction. The remaining blocks perform all the essential operations of the ADC. First, 15 comparators sample the data (replacing the T/H), amplify it (replacing the preamplifiers), and have built-in threshold levels (replacing the reference ladder). Second, the outputs of the comparators are stored in 15 Set-Reset latches. Next, a ROM-based encoder converts the stored thermometer code into a 4b Gray code that has intrinsic error correcting properties. The word-line selection of the encoder is performed by an array of 2-input NAND gates that detect the 0 to 1 crossing of the thermometer code. The clock circuit generates non-overlapping clocks for the dynamic-logic encoder and comparators. The comparator circuit combines its three functions (sampling, amplification, and generating reference levels) with high accuracy and high sampling speed at low power. It is the critical block of this architecture. To implement this functionality a dynamic comparator based on [5] with calibration is designed. The calibration data of the comparators is stored in a shift register.

The comparator consists of an input differential pair feeding a current in a regenerative cross-coupled pair (Fig. 31.1.2). The cross-coupled pair provides a large gain and if given sufficient time it will amplify any differential input signal into full logic levels. The time for this amplification is expressed as the required number of time constants of the regenerative loop. With the high f_T of the 90nm process used for the implementation of this ADC, even at the high sampling rate of 1.25GS/s, at least 15 times of the time constant of the regenerative loop is available to determine the sign of the input signal. To implement the reference levels an intentional imbalance has been introduced in the input differential pair. This causes the trip point of the comparator to shift by an amount given by:

$$\Delta V_{level\ i} = \frac{i * \Delta W}{W} \frac{I_{M1}}{g_{m,M1}} \approx \frac{i * \Delta W}{W} \frac{V_{gs,M1} - V_T}{2}$$

where i varies from –7 to 7 for the 15 reference levels.

To lower the power consumption of the comparator the sizes of the transistors are minimized at the expense of an increased level of mismatch. To compensate for the mismatch errors, calibration devices are added. Unlike other implementations that apply a static correction using, e.g., current sources, this circuit uses a dynamic correction with capacitors as in [6]. A binary-scaled array of variable capacitors is added to the output nodes of the input differential pair (see Fig. 31.1.2). A different capacitive load at these nodes requires a difference in current (dis)charging these nodes, which effectively shifts the comparator's input threshold voltage. The amount of threshold shift is given by:

$$\Delta V_{threshold} = \frac{\Delta C_{\text{varicap}}}{C_{total}} \frac{I_{M1}}{g_{m,M1}} \approx \frac{\Delta C_{\text{varicap}}}{C_{total}} \frac{V_{gs,M1} - V_T}{2}.$$

The loading of this additional capacitance slows down the comparator but the key is to make this additional capacitance as small as possible. The slow down is then minor and the threshold can be tuned very accurately. The small variable capacitor devices are implemented using PMOS transistors, with the source/drain side connected to the comparator node and the gate node controlling the value of the capacitance: when 0V is applied to the gate of this device a channel is created and the oxide capacitance is added to the comparator node, when 1.2V is applied to the gate no channel is present. The threshold can be shifted in 3mV steps, that is much smaller than the LSB resolution of 12.5mV.

The chip (Fig. 31.1.7) is fabricated in a 90nm CMOS process. For this design only NMOS (V_T is 0.3V) and PMOS (V_T is -0.3V) transistors are used. The NMOS device has a maximum g_m of 1250mS/mm width, and a maximum f_T of 150GHz. The chip, including all the blocks of Fig. 31.1.1, draws 2.1 mA from a 1.2V supply.

The calibration of the threshold voltages is performed with DC input signals, and is sufficiently accurate to reduce the INL to less than 0.15LSB (Fig. 31.1.3). This calibration is performed at a low operating speed (50MS/s) and downloaded to the chip for the remainder of the measurements. The chip is then clocked at 1.25GS/s and a full-scale input signal with varying frequency is applied (Fig. 31.1.4). The SNDR at low frequencies is 24dB which corresponds to an ENOB of 3.7. This SNDR remains at 23.8dB at the Nyquist frequency. The output spectrum of an input signal at 640MHz is shown in Fig. 31.1.5 indicating an SFDR of 35dB. The ERBW, frequency at which the ENOB drops by 0.5b, extends up to 3.3GHz. This shows the dynamic performance is not adversely affected by the absence of the T/H, preamplifier, and bubble error correction circuits. All performance values are summarized in Fig. 31.1.6.

For the purpose of performance comparison with other state-of-the-art implementations a FOM of $\frac{P}{2^{ENOB} \times 2 \times f_{in}}$ as in [2] is used. For f_{in} equal to the Nyquist frequency (f_{in}=625MHz) a 0.16pJ/conversion-step is achieved. Other comparable designs have FOMs between 0.5 to 10pJ [2, 3, 4].

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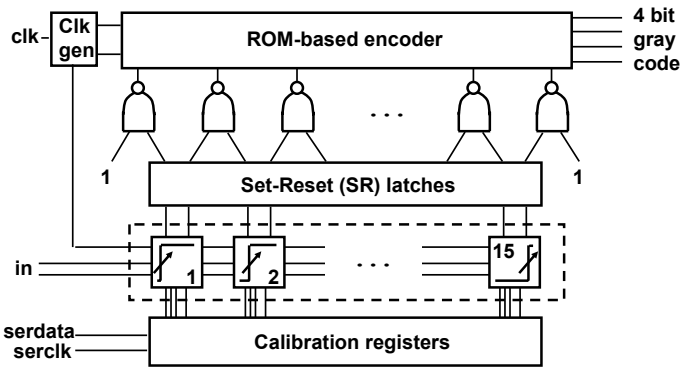

Figure 31.1.1: Architecture of the 4b flash ADC.

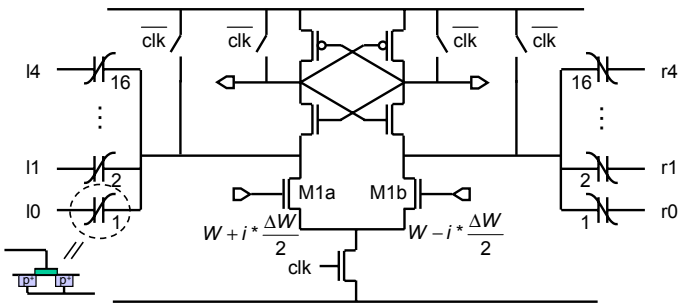

Figure 31.1.2: Dynamic comparator with built-in reference levels and dynamic calibration.

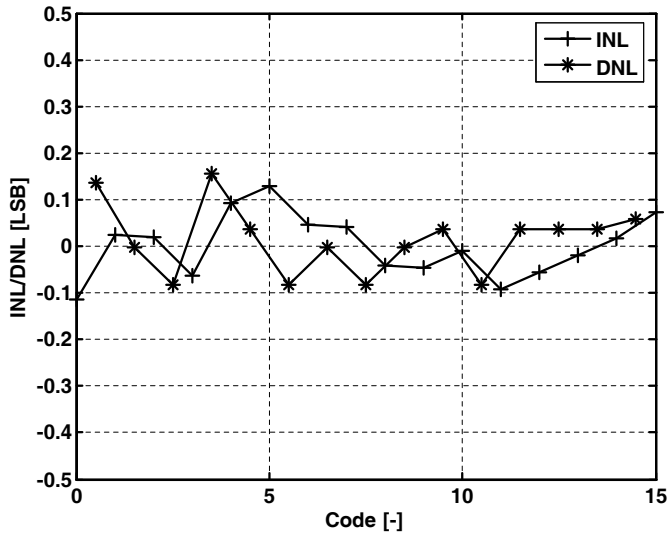

Figure 31.1.3: INL and DNL of converter after calibration.

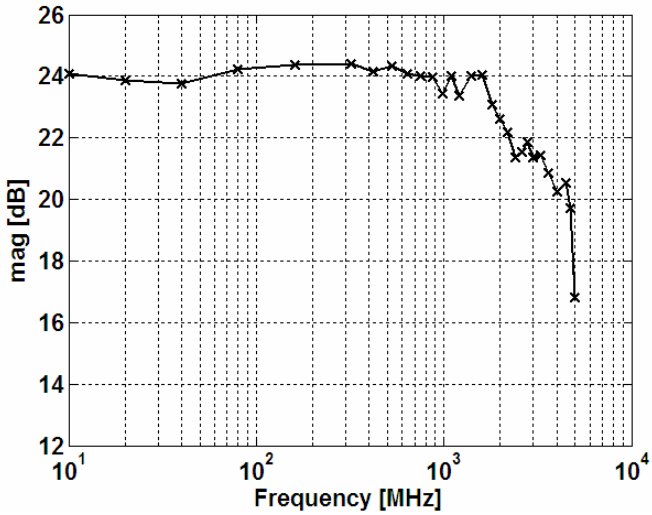

Figure 31.1.4: SNDR versus f_{in} at f_{clk}=1.25GS/s.

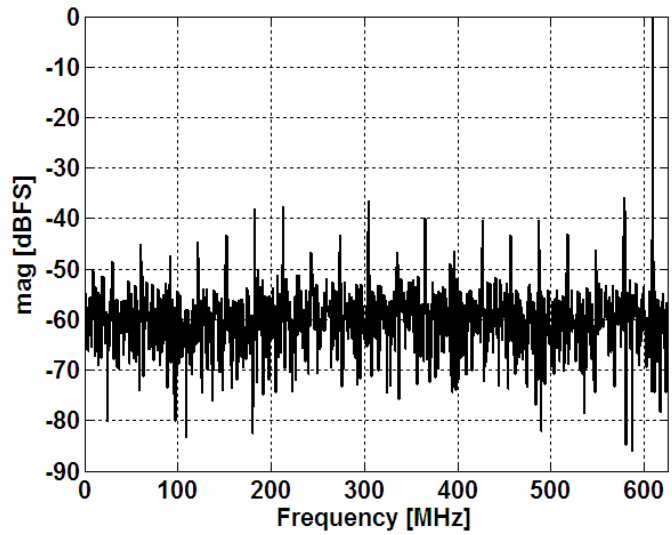

Figure 31.1.5: Output spectrum when f_{in}=640MHz and f_{clk}=1.25GS/s.

Technology	90 nm CMOS 1P5M Cu-metal	
Input range	200	$mV_{ptp,diff}$
DNL	< 0.2	LSB
INL	< 0.15	LSB
ENOB @ DC	3.7	bit
Input capacitance	70	fF
SNDR @ Nyquist	23.8	dB
Sampling frequency	1.25	GS/s
ERBW	3.3	GHz
Latency	1	Clock cycle
Supply Voltage	1.2	V
Power	2.5	mW
Area (w/o decoupling)	300 x 110	µm

Figure 31.1.6: Performance summary.

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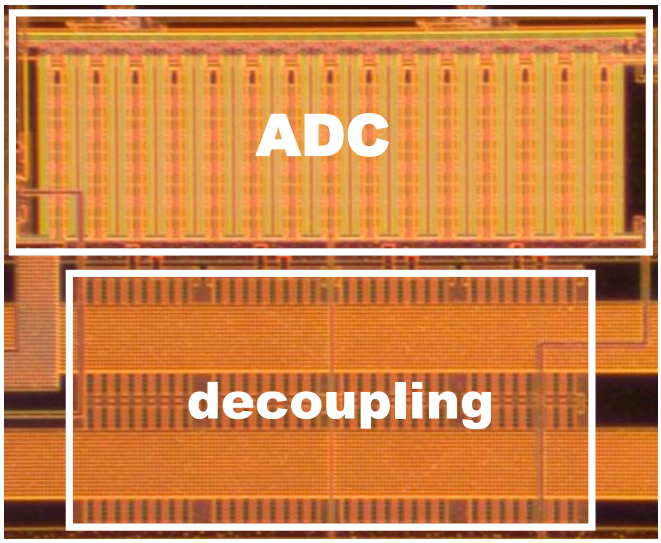

Figure 31.1.7: Chip micrograph of the 90nm CMOS 4b ADC.

